General Information

MATERIALS EXPERT

For 50 years and as a market leader, EXXELIA's comprehensive knowledge of the materials properties and performances have enabled us to design capacitors in Porcelain, NP0, BX, 2C1, BP, X7R and -2200ppm/° C ceramics.

CUSTOM DESIGNS

Our catalog products don't meet your application?

Based on the valuable experience accumulated over the design of 2,000+ specific ceramic capacitors, you can trust EXXELIA to define a qualitative custom solution in a time effective manner.

NO OBSOLESCENCE

Choosing a standard or custom Exxelia product means you won't have to worry about obsolescence.

TYPICAL APPLICATIONS

- Aerospace & Defense: cockpit panels, flight control, radio systems, missile guidance systems…
- Space: military and commercial satellites, launcher…
- Medical: MRI, external defibrillators, implantable devices…
- Telecommunications: base stations…
- Oil and gas: drilling tools, MWD, LWD, wellheads…

ISO 9001 AND AS9100C

Quality is at the core of Exxelia's corporate culture. Each sites has its own certifications.

CERTIFICATIONS

Capacitors manufactured by EXXELIA comply with American and European standards and meet the requirements of many international standards.
For Space qualified parts (ESA QPL), please refer to our catalog «Ceramic capacitors for Space applications».

QUALITY & RELIABILITY

EXXELIA is committed to design and manufacture high quality and reliability products. The test cycles reproducing the most adverse operating conditions over extended periods (up to 10 000 hours) have logged to date well over 5.109 hours/°Component.
Failure rate data can be provided upon request.

CONFLICT MINERALS

EXXELIA is committed to an approach based on «Conflict Minerals Compliance». This US SEC rule demands complete traceability and a control mechanism for the mineral procurement chain, encouraging importers to buy only «certified» ore.
We have discontinued relations with suppliers that procure from the Democratic Republic of the Congo or an adjoining country.

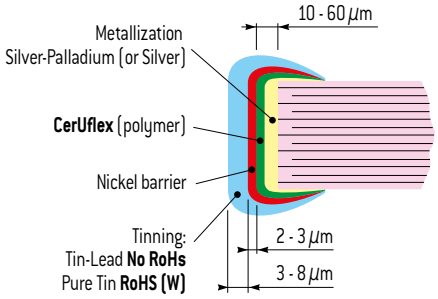
ENVIRONMENT

EXXELIA is committed to applying a robust environmental policy, from product design through to shipment. To control its environmental footprint and reconcile this with the company' functional imperatives, our environmental policy provides for the reduction or elimination of hazardous substances. We also focus on compliance with European Union directives and regulations, notably REACH and RoHS.

RoHS COMPLIANCY

SMD CAPACITORS

The capacitor terminations are generally protected by a nickel barrier formed by electrolytic deposit. This barrier gives chip capacitors leaching performance far exceeding the requirements of all applicable standards. The nickel barrier guarantees a minimum resistance to soldering heat for a period of 1 minute at 260°C in a tin-lead (60/40) or tin-lead-silver (62/36/2) bath without noticeable alteration to the solderability. It also allows repeated soldering-unsoldering and the longer soldering times required by reflow techniques.
However nickel barrier amplifies thermal shock and is not recommended for chip sizes equal or greater than CNC Y (30 30) - (C 282 to C 288 - CNC 80 to CNC 94).

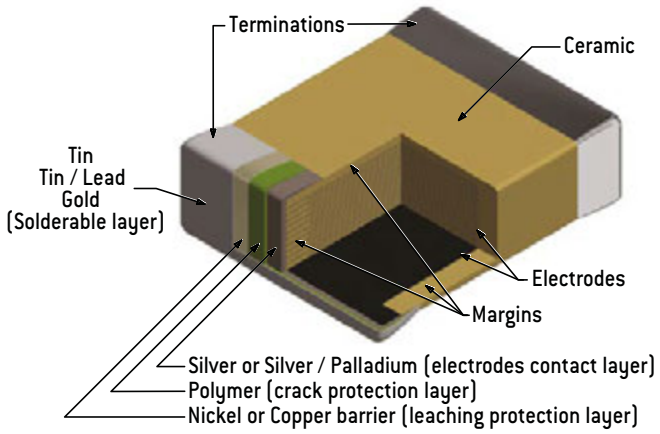


LEADED COMPONENTS

As well as for SMD products, leaded capacitors ranges can also be RoHS. These products, which are characterized by the suffix «W» added to the commercial type, are naturally compatible with the soldering alloys used in RoHS mounting technology. The connections coating is generally an alloy SnAg (with a maximum of 4% Ag). However, on a few products that Exxelia will precise on request, the coating is pure silver.

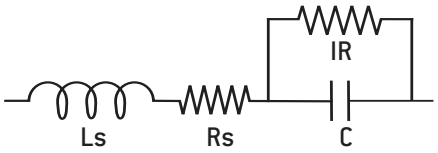
Ceramic Capacitors Technology

MLCC STRUCTURE



EQUIVALENT CIRCUIT

Capacitor is a complex component combining resistive, inductive and capacitive phenomena. A simplified schematic for the equivalent circuit is:



DIELECTRIC CHARACTERISTICS

Insulation Resistance (IR) is the resistance measured under DC voltage across the terminals of the capacitor and consists principally of the parallel resistance shown in the equivalent circuit. As capacitance values and hence the area of dielectric increases, the IR decreases and hence the product (C x IR) is often specified in Ω.F or MΩ.μF.

The Equivalent Series Resistance (ESR) is the sum of the resistive terms which generate heating when capacitor is used under AC voltage at a given frequency (f).

Dissipation factor (DF) is the ration of the apparent power input will turn to heat in the capacitor:

$DF = 2\pi f C ESR$

When a capacitor works under AC voltage, **heat power loss (P),** expressed in Watt, is equal to:

$P = 2\pi f C Vrms^2 DF$

The series inductance (Ls) is due to the currents running through the electrodes. It can distort the operation of the capacitor at high frequency where the **impedance (Z)** is given as:

$Z = Rs + j (Ls.\omega - 1/(C.\omega))$ with $\omega = 2\pi f$

When frequency rises, the capacitive component of capacitors is gradually canceled up to the resonance frequency, where :

$Z = Rs$ and $LsC.\omega^2 = 1$

Above this frequency the capacitor behaves like an inductor.

	P100	NP0	N2200 (C4xx)	BX	2C1	X7R
Dielectric material	Porcelain	Magnesium titanate or Neodynium baryum titanate	Barium zirconate titanate	Baryum titanate ($BaTiO_3$)		
Dielectric constant	15 – 18	20 – 85	450	2,000 – 5,000		
Electrode technology	PME (Precious Metal Electrodes): Ag/Pd					
Capacitance variation between –-55°C and +125/° C without DC voltage	(100±30)ppm/° C	(0±30)ppm/° C	(–2,200±500) ppm/° C	±15%	±20%	±15%
Capacitance variation between –-55°C and +125/° C with DC rated voltage			0 -15%	15% –25%	20% –30%	Not applicable
Piezo-electric effect	None		None	Yes		
Dielectric absorption	None		Few %	Few %		
Thermal shock sensitive	+		+	++		

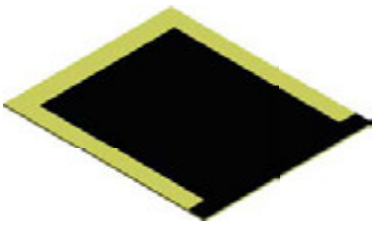
Ceramic Capacitors Technology

MANUFACTURING STEPS

SLIP CASTING

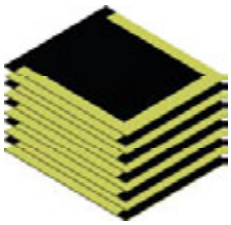
A slurry, a mix of ceramic powder, binder and solvents, is poured onto conveyor belt inside a drying oven, resulting in a dry ceramic sheet.

ELECTRODE SCREEN PRINTING



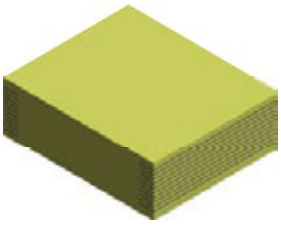
The electrode ink, made from a metal powder mixed with solvents, is printed onto the ceramic sheets using a screen printing process.

STACKING



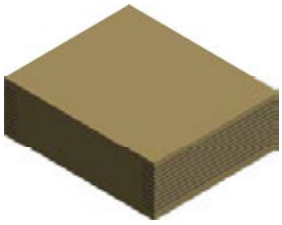
The sheets with electrode printed are stacked to create a multilayer structure.

PRESSING



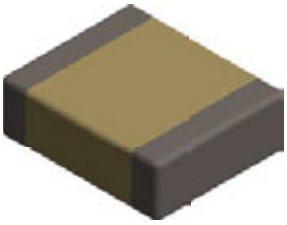
Pressure is applied to the stack to fuse all the separate layers, this created a monolithic structure.

SINTERING



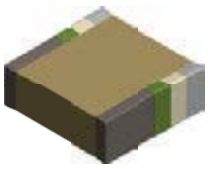
The parts are sintered in an oven with a precise temperature profile which is very important to the characteristics of the capacitors.

TERMINATIONS



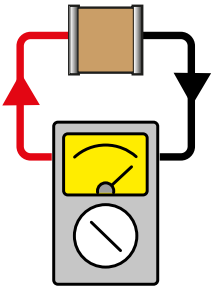
Each terminal of the capacitor is dipped in the termination ink, mix of metal powder, solvents and glass frit and the parts are fired in an oven.

TERMINATIONS PLATING



Stacking + leads soldering + encapsulation
(see pages 10-11)

FINAL TESTING



PACKAGING

User Guide

SMD TERMINATIONS

NON RoHS COMPLIANT	Code	RoHS COMPLIANT	Code	Magnetic	Recommended mounting process						Storage (months)*
					Epoxy bonding	Iron soldering	Wave soldering	Vapor phase soldering	Infrared soldering	Wire bonding	
Ag	**Q**	Ag	**QW / P**	No	●	●	●	●			18
Ag/Pd/Pt	**-**	Ag/Pd/Pt	**W / A**	No	●	●	●				24
Ag + Ni + dipped Sn/Pb 60/40	**T****	-	**-**	No		●	●	●	●		24
Ag/Pd/Pt + dipped Sn/Pb 60/40	**H**	Ag/Pd/Pt + dipped Sn	**HW**	No		●					24
Ag + Ni + electrolytic Sn/Pb 95/5	**C**	Ag + Ni + electrolytic Sn	**CW / S**	Yes		●	●	●	●		18
Ag + Ni + electrolytic Sn/Pb 60/40	**D**	-	**-**	Yes		●	●	●	●		18
-	**-**	Ag + Cu + electrolytic Sn	**C*****	No		●	●	●	●		18
Ag + Ni + dipped Sn/Pb 60/40	**E**	Ag + Ni + electrolytic Sn	**EW**	Yes		●	●				24
Ag + Ni + Au	**G**	Ag + Ni + Au	**GW**	Yes	●	●	●	●	●	●	36
Ag + Polymer + Ni + Sn/Pb 95/5	**YC**	Ag + Polymer + Ni + Sn	**YCW**	Yes		●	●	●	●		18
Ag + Polymer + Ni + Sn/Pb 60/40	**YD**	-	**-**	Yes		●	●	●	●		18
Ag + Polymer + Ni + Au	**YG**	Ag + Polymer + Ni + Au	**YGW**	Yes	●	●	●	●	●	●	36

Nickel (Ni) or Copper (Cu) barriers amplify thermal shock and are not recommended for chip sizes larger than 3030.

* Storage must be in a dry environment at a temperature of 20° C with a relative humidity below 50%, or preferably in a package enclosing a desiccant.
** Maintenance only.
*** Non magnetic chips series only.

SMD ENVIRONMENTAL TESTS

Ceramic chip capacitors for SMD are designed to meet test requirements of **CECC 32100** and **NF C 93133** standards as specified below in compliance with NF C 20700 and IEC 68 standards:

- Solderability: **NF C 20758,** 260° C, bath 62/36/2.
- Adherence: 5N force.
- Vibration fatigue test: **NF C 20706,** 20 g, 10 Hz to 2,000 Hz, 12 cycles of 20 minutes each.
- Rapid temperature change: **NF C 20714,** – –55°C to + 125° C, 5 cycles.
- Combined climatic test: **IEC 68-2-38.**
- Damp heat: **NF C 20703,** 93 %, H.R., 40° C.
- Endurance test: 1,000 hours, 1.5 U_{RC}, 125° C.

STORAGE OF CHIP CAPACITORS

TINNED OR NON TINNED CHIP CAPACITORS

Storage must be in a dry environment at a temperature of 20°C with a relative humidity below 50 %, or preferably in a packaging enclosing a desiccant.

STORAGE IN INDUSTRIAL ENVIRONMENT:

- 2 years for tin dipped chip capacitors,
- 18 months for tin electroplated chip capacitors,
- 2 years for non tinned chip capacitors,
- 3 years for gold plated chip capacitors.

STORAGE IN CONTROLLED NEUTRAL NITROGEN ENVIRONMENT:

- 4 years for tin dipped or electroplated chip capacitors,
- 4 years for non tinned chip capacitors,
- 5 years for gold plated chip capacitors.

Storage duration should be considered from delivery date and not from batch manufacture date. The tests carried out at final acceptance stage (solderability, susceptibility to solder heat) enable to assess the compatibility to surface mounting of the chips.

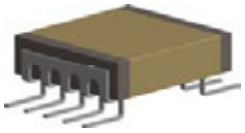
LEAD STYLES

SURFACE MOUNTING

DIL LEADS

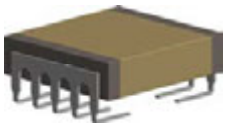
P style

PL style



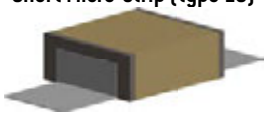
L style

J style

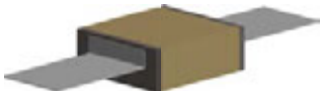


RIBBON LEADS

Micro-strip (type 1)
Short Micro-strip (type 1S)

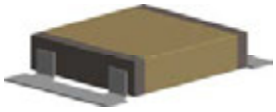


Axial (Type 2)

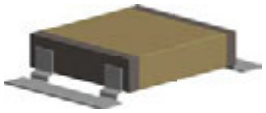


Radial (Type 3)

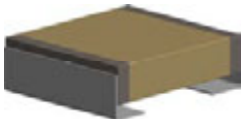
R style



RX style



RJ style



Please contact Exxelia sales for any lead configuration not shown.

TROUGH-HOLE MOUNTING

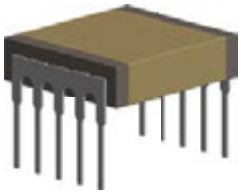
AXIAL AND RADIAL

Radial leads (Type 6)

Radial leads (4 leads)

Axial leads (Type 7)

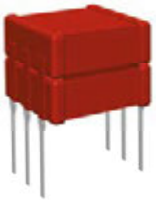
DIL leads: N style



ENCAPSULATION STYLES

Ceramic encapsulation
(selfprotected)

Varnish

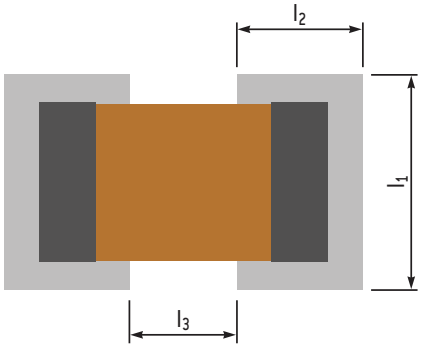


Conformal coating

Molding

User Guide

SOLDERING ADVICES FOR REFLOW SOLDERING



Large chips above size 2225 are not recommended to be mounted on epoxy board due to thermal expansion coefficient mismatch between ceramic capacitor and epoxy. Where larger sizes are required, it is recommended to use components with ribbon or other adapted leads so as to absorb thermo-mechanical strains.

Dimensions in inches (in mm)	Reflow soldering						Wave soldering					
	I_1		I_2		I_3		I_1		I_2		I_3	
0402	0.043	(1.1)	0.035	(0.9)	0.012	(0.3)	0.043	(1.1)	0.047	(1.2)	0.012	(0.3)
0403	0.055	(1.4)	0.035	(0.9)	0.012	(0.3)	0.055	(1.4)	0.047	(1.2)	0.012	(0.3)
0504	0.063	(1.6)	0.051	(1.3)	0.016	(0.4)	0.063	(1.6)	0.063	(1.6)	0.016	(0.4)
0603	0.055	(1.4)	0.059	(1.5)	0.02	(0.5)	0.055	(1.4)	0.071	(1.8)	0.02	(0.5)
0805	0.073	(1.85)	0.065	(1.65)	0.024	(0.6)	0.073	(1.85)	0.077	(1.95)	0.024	(0.6)
0907	0.094	(2.4)	0.065	(1.65)	0.035	(0.9)	0.094	(2.4)	0.077	(1.95)	0.035	(0.9)
1005	0.073	(1.85)	0.067	(1.7)	0.039	(1)	0.073	(1.85)	0.079	(2)	0.039	(1)
1206	0.083	(2.1)	0.067	(1.7)	0.059	(1.5)	0.083	(2.1)	0.079	(2)	0.059	(1.5)
1210	0.118	(3)	0.069	(1.75)	0.059	(1.5)	0.118	(3)	0.081	(2.05)	0.059	(1.5)
1605	0.073	(1.85)	0.071	(1.8)	0.087	(2.2)	0.073	(1.85)	0.083	(2.1)	0.087	(2.2)
1806	0.087	(2.2)	0.073	(1.85)	0.102	(2.6)	0.087	(2.2)	0.085	(2.15)	0.102	(2.6)
1812	0.152	(3.85)	0.073	(1.85)	0.102	(2.6)	0.152	(3.85)	0.085	(2.15)	0.102	(2.6)
1825	0.281	(7.15)	0.073	(1.85)	0.102	(2.6)	0.281	(7.15)	0.085	(2.15)	0.102	(2.6)
2210	0.13	(3.3)	0.079	(2)	0.146	(3.7)	0.13	(3.3)	0.091	(2.3)	0.146	(3.7)
2220	0.228	(5.8)	0.079	(2)	0.146	(3.7)	0.228	(5.8)	0.091	(2.3)	0.146	(3.7)
2225	0.281	(7.15)	0.079	(2)	0.146	(3.7)	0.281	(7.15)	0.091	(2.3)	0.146	(3.7)

RECOMMENDED FOOTPRINT FOR SMD CAPACITORS

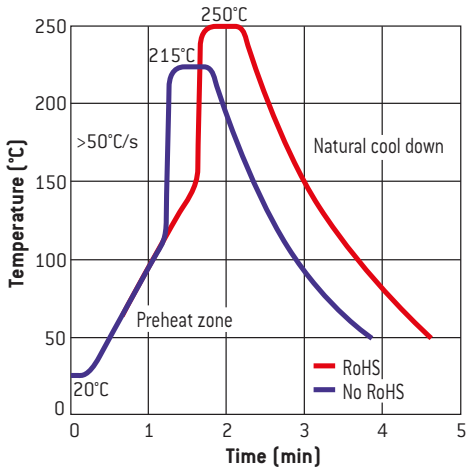
Ceramic is by nature a material which is sensitive both thermally and mechanically. Stresses caused by the physical and thermal properties of the capacitors, substrates and solders are attenuated by the leads.

Wave soldering is unsuitable for sizes larger than 2220 and for the higher ends of capacitance ranges due to possible thermal shock (capacitance values given upon request).

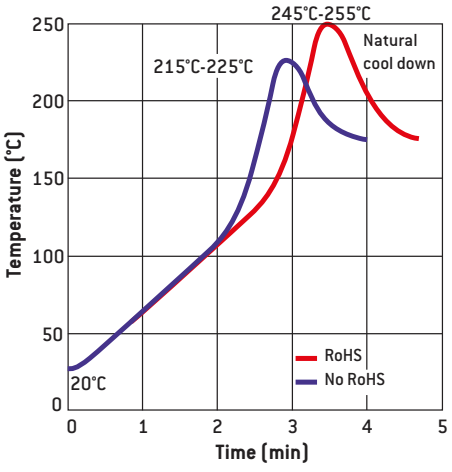
Infrared and vapor phase reflow, are preferred for high reliability applications as inherent thermo-mechanical strains are lower than those inherent to wave soldering.

Whatever the soldering process is, it is highly recommended to apply a thermal cycle, see hereafter our recommended soldering profile:

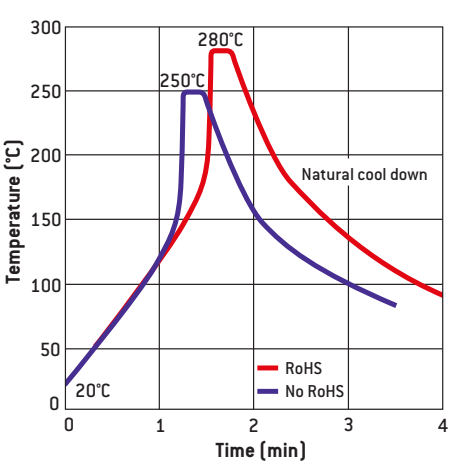
RECOMMENDED VAPOR PHASE REFLOW PROFILE



RECOMMENDED IR REFLOW PROFIL



RECOMMENDED WAVE SOLDERING PROFILE



SOLDERING ADVICES FOR IRON SOLDERING

Attachment with a soldering iron is discouraged due to ceramic brittleness and the process control limitations. In the event that a soldering iron must be used, the following precautions should be observed:

- Use a substrate with chip footprints big enough to allow putting side by side one end of the capacitor and the iron tip without any contact between this tip and the component,
- place the capacitor on this footprint,
- heat the substrate until the capacitor's temperature reaches 150° C minimum (preheating step, maximum 1°C per second),
- place the hot iron tip (a flat tip is preferred) on the footprint **without touching the capacitor.** Use a regulated iron with a 30 watts maximum power. The recommended temperature of the iron is 270 ±10° C. The temperature gap between the capacitor and the iron tip must not exceed 120° C,
- leave the tip on the footprint for a few seconds in order to increase locally the footprint's temperature,
- use a cored wire solder and put it down on the iron tip. In a preferred way use Sn/Pb/Ag 62/36/2 alloy,
- wait until the solder fillet is formed on the capacitor's termination,
- take away iron and wire solder,
- wait a few minutes so that the substrate and capacitor come back down to the preheating temperature,
- solder the second termination using the same procedure as the first,
- let the soldered component cool down slowly to avoid any thermal shock.

PACKAGING

TAPE AND REEL

The films used on the reels correspond to standard IEC 60286-3. Films are delivered on reels in compliance with document IEC 286-3 dated 1991.

Minimum quantity is 250 chips.

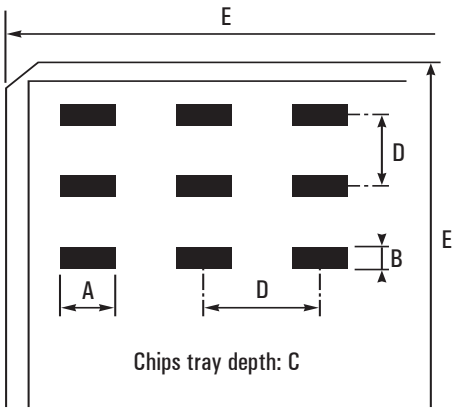
Maximum quantities per reel are as follows:

- Super 8 reel - Ø 180: 2,500 chips.
- Super 8 reel - Ø 330: 10,000 chips.
- Super 12 reel - Ø 180: 1,000 chips.

Reel marking complies with CECC 32100 standard:

- Model.
- Rated capacitance.
- Capacitance tolerance.
- Rated voltage.
- Batch number.

TRAY PACKAGES



DIMENSIONAL CHARACTERISTICS OF CHIPS TRAY PACKAGES

Sizes	Nr. of chips/ package	Oriented chips	Dimensions in inches (in mm)				
			A	B	C	D	E
0402	100	No	Ø 0.112 (Ø 3.02)		0.065 (1.65)	0.167 (4.24)	2 (50.8)
0403	100	No	Ø 0.112 (Ø 3.02)		0.065 (1.65)	0.167 (4.24)	2 (50.8)
0504	100	Yes	0.059 (1.5)	0.045 (1.14)	0.035 (0.89)	0.167 (4.24)	2 (50.8)
0603	340	Yes	0.1 (2.54)	0.06 (1.52)	0.045 (1.14)	0.167 (4.24)	2 (50.8)
0805	100	Yes	0.1 (2.54)	0.06 (1.52)	0.045 (1.14)	0.167 (4.24)	2 (50.8)
1206	100	No	0.14 (3.56)	0.14 (3.56)	0.06 (1.52)	0.167 (4.24)	2 (50.8)
1210	100	Yes	0.14 (3.56)	0.14 (3.56)	0.06 (1.52)	0.167 (4.24)	2 (50.8)
1812	100	No	0.25 (6.35)	0.25 (6.35)	0.13 (3.3)	0.345 (8.76)	4 (101.6)
	25	Yes	0.24 (6.1)	0.265 (6.73)	0.07 (1.78)	0.345 (8.76)	2 (50.8)
2220	100	Yes	0.25 (6.35)	0.25 (6.35)	0.13 (3.3)	0.345 (8.76)	4 (101.6)
	25	Yes	0.24 (6.1)	0.265 (6.73)	0.07 (1.78)	0.345 (8.76)	2 (50.8)

User Guide

EIA STANDARD CAPACITANCE VALUES

Following EIA standard, the values and multiples that are indicated in the chart below can be ordered. E48, E96 series and intermediary values are available upon request.

E6 (± 20%)	E12 (± 10%)	E24 (± 5%)
10	10	10
		11
	12	12
		13
15	15	15
		16
	18	18
		20
22	22	22
		24
	27	27
		30
33	33	33
		36
	39	39
		43
47	47	47
		51
	56	56
		62
68	68	68
		75
	82	82
		91

PART MARKING VOLTAGE CODES

Use the following voltage code chart for part markings:

Voltage (V)	Code	Letter code
25	250	A
40	400	B
50	500	C
63	630	D
100	101	E
200	201	G
250	251	H
400	401	K
500	501	L
1,000	102	M
2,000	202	P
3,000	302	R
4,000	402	S
5,000	502	T
7,500	752	U
10,000	103	W

EIA CAPACITANCE CODE

The capacitance is expressed in three digit codes and in units of pico Farads (pF). The first and second digits are significant figures of the capacitance value and the third digit identifies the multiplier.

For capacitance value < 10pF, R designates a decimal point.
See examples below:

EIA code	Capacitance value		
	in pF	in nF	in µF
2R2	2.2	0.0022	0.0000022
6R8	6.8	0.0068	0.0000068
220	22	0.022	0.000022
470	47	0.047	0.000047
181	180	0.18	0.00018
221	220	0.22	0.00022
102	1,000	1	0.001
272	2,700	2.7	0.0027
123	12,000	12	0.012
683	68,000	68	0.068
124	120,000	120	0.12
564	560,000	560	0.56
335	3,300,000	3,300	3.3
825	8,200,000	8,200	8.2
156	15,000,000	15,000	15
686	68,000,000	68,000	68
107	100,000,000	100,000	100
227	220,000,000	220,000	220

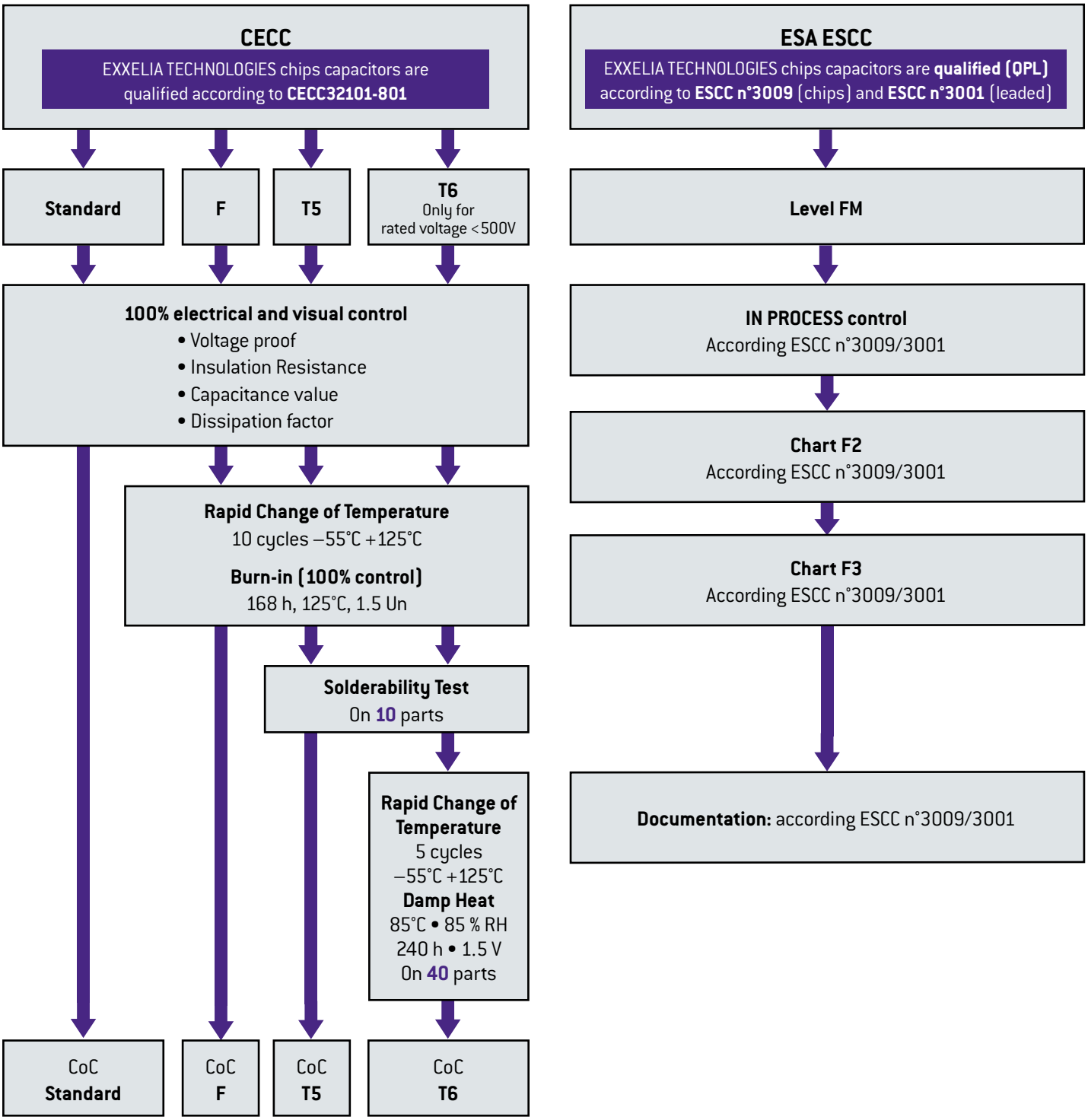
PART MARKING TOLERANCE CODES

Use the following tolerance code chart for part markings:

Tolerance	Letter code
±0.25pF	CU
±0.5pF	DU
±1pF	FU
±1%	F
±2%	G
±5%	J
±10%	K
±20%	M

RELIABILITY LEVELS

Exxelia proposes different reliability levels for the ceramic capacitors for both NP0 and X7R ceramics.



Custom Design

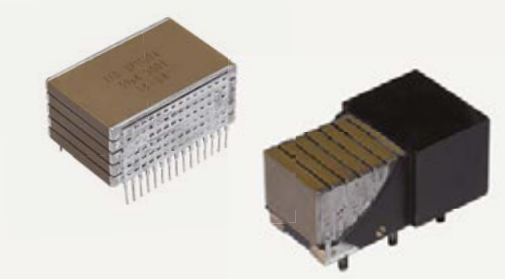
As the world's leading manufacturer of specific passive components, we stand apart through our ability to quickly evaluate the application specific engineering challenges and provide a cost-effective and efficient solutions.

For requirements that cannot be met by catalog products, we offer leading edge solutions in custom configuration: custom geometries, packaging, characteristics, all is possible thanks to our extensive experience and robust development process, while maintaining the highest level of reliability.

Where necessary, special testing is done to verify requirements, such as low dielectric absorption, ultra-high insulation resistance, low dissipation factor, stability under temperature cycling or under specified environmental conditions, etc.

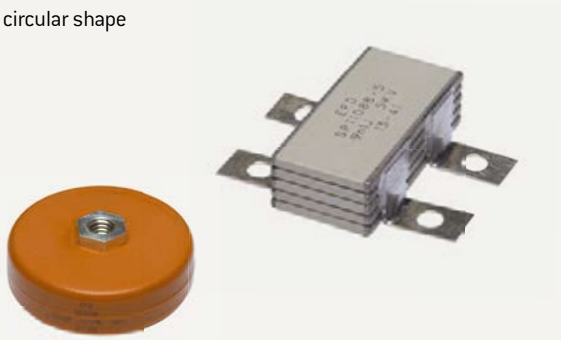
HIGH CAPACITANCE

- High energy density
- Specific case sizes
- Specific shape of connections (high resistance to vibrations)



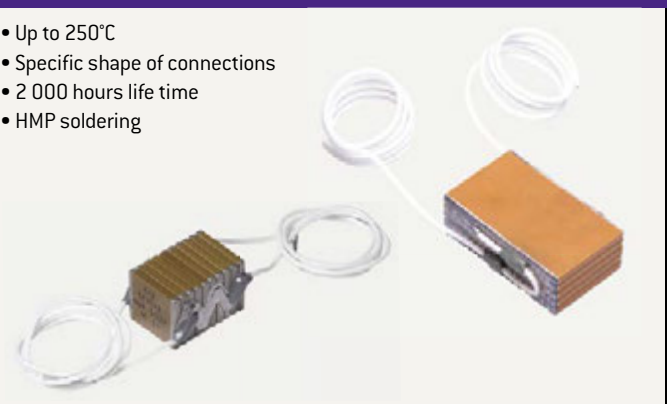
HIGH VOLTAGE

- Up to 50 kV
- Specific circular shape



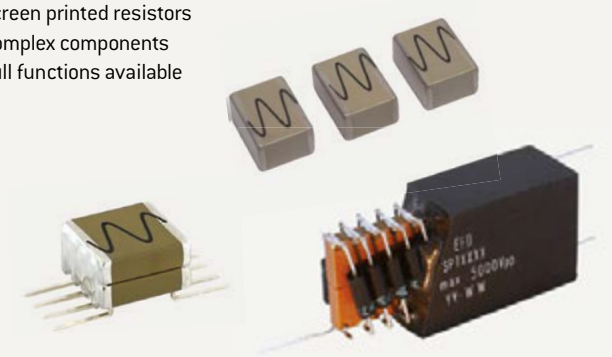
HIGH TEMPERATURE

- Up to 250°C
- Specific shape of connections
- 2 000 hours life time
- HMP soldering



OTHERS

- Screen printed resistors
- Complex components
- Full functions available



General Information

CAPACITOR TERMINATIONS AND SOLDERING RECOMMENDATIONS

I. TERMINATION TYPES

Our capacitors are delivered with one of the following terminations (for technical reasons, only a limited number of termination types are available in certain cases). All our terminations are backward compatible.

Parameter	Value	Comment
Termination Materials	A	non-magnetic (silver-palladium)
	C	non-magnetic (pure tin over copper barrier)
	S	lead-free (pure tin over nickel barrier)

NB:

- terminations type C recommended for non magnetic applications.
- termination type A available for non magnetic applications (for historical reason, we have also another code, the code "P", for the same type of termination. The parts that were designed-in before 2005 might still have a code "P" instead of "A" in the part numbering. But both codes correspond to the same type of termination).

II. SPECIFICATIONS

Care must be taken when using particular terminations: if the terminations are heated up above a particular temperature and/or for too long a period of time, there is a risk of leaching (dissolution of the termination revealing the inner electrodes).

The chart below gives the resistance to soldering heat per termination type, based on a SAC387 solder bath at 260°C.

Dielectric Type	A	C	S
CHA / SHA		10 $\pm$1s (3)	120 $\pm$5s
CHB / SHB		30 $\pm$2s	120 $\pm$5s
CPX / CLX / CPE / CLE		30 $\pm$2s	120 $\pm$5s
CLF	10 $\pm$2s (1)	On request	120 $\pm$5s
SHL			120 $\pm$5s
SHS		10 $\pm$1s (4)	120 $\pm$5s
SHF / SHN / SHT	5 $\pm$1s (2)		120 $\pm$5s

(1): results extrapolated from 30 $\pm$ 2s data obtained with Sn62/Pb36/Ag2 solder bath.
(2): data obtained with Sn62/Pb36/Ag2 solder bath.
(3): termination only available on CHA series.
(4): preliminary data.

III. STANDARD SMD REQUIREMENTS

III.1. Soldering Recommendations

Regarding the soldering attachments, three methods are generally used: the vapor phase soldering, the infrared reflow soldering and the wave soldering. Unless particular skill about the use of the wave soldering, this method is not recommended since the melted solder is directly in contact with the ceramic. This can potentially crack the capacitor because the ceramic is sensible to the thermal shocks. Moreover, this method needs to maintain the components with an insulating resin which increases the thermo-mechanical strains between the ceramic and the board both on soldering phase and operating condition. The vapour phase and IR reflow soldering are less aggressive, inducing more restricted thermal shocks. This is the reason why they are preferred to the wave soldering method for reliable applications. In all cases, proper pre-heating is essential.

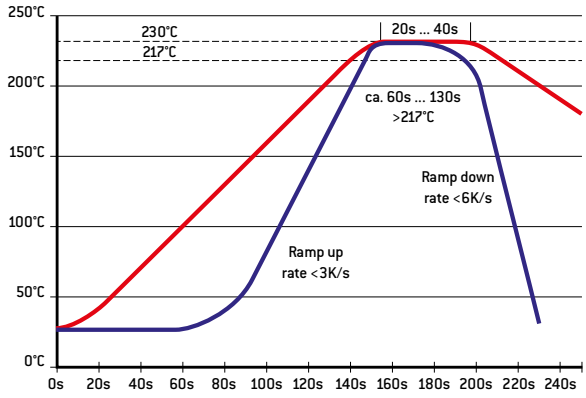
The circuit should be pre-heated at a typical rate of 1°C/s within 65°C to 100°C of the maximum soldering temperature. While multilayer ceramic capacitors can withstand the peak soldering temperatures for short durations, they should be minimized whenever possible.

Above precaution given for SMD types are applicable for the implementation of large bare chips (1515 and above). But in general, large bare chips above 2225 are not recommended to be mounted on epoxy printed board due to the thermal expansion mismatch between ceramic capacitor body and epoxy. This is the reason why leaded components will be preferred especially for reliable applications.

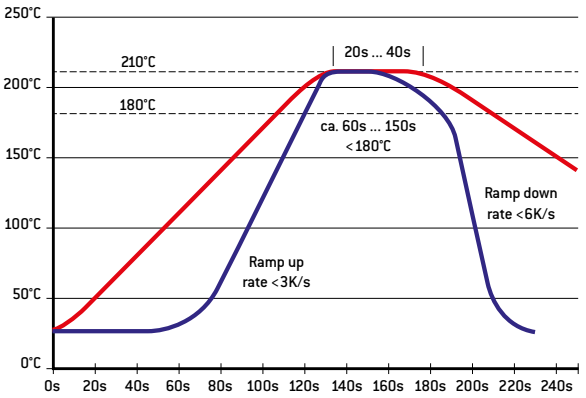
For information, the typical thermal profiles of these three soldering processes are given hereafter. These typical diagrams are only given as an aid to SMD users in determining specific processes linked to their instrumentations and to their own experience.

NB: reference documents are IEC 61760-1, CECC30000 and IEC68 standards. Please, refer to this standard for more information.

III.1.1. Vapour Phase Soldering



Lead free SnAgCu solders - Vapour Phase

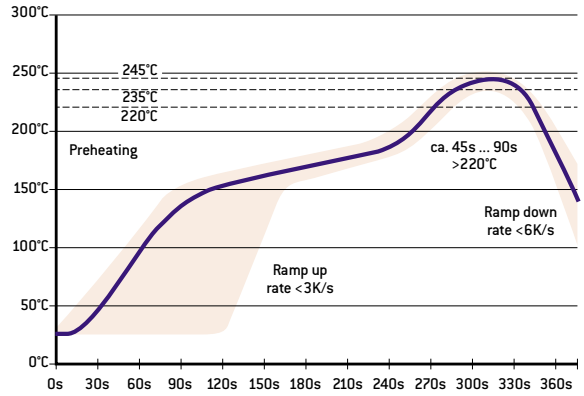


SnPb solders – Infrared Soldering

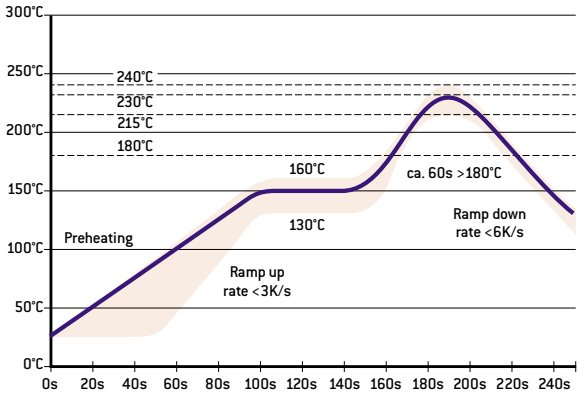
NB: the lines indicate the upper and lower limits of typical process (terminal temperature).

General Information

III.1.2. Infrared Soldering



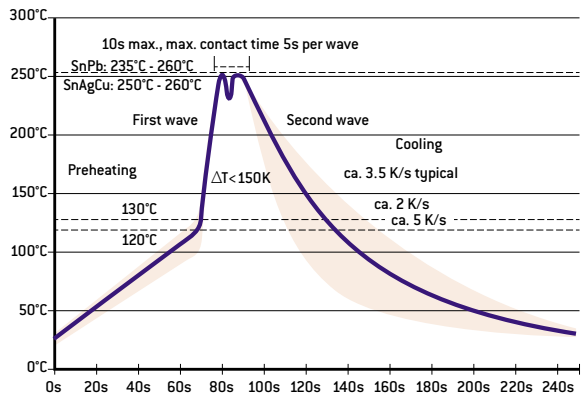
Lead free SnAgCu solders – Infrared Soldering



SnPb solders – Infrared Soldering

NB:
- these profiles are given for mid size components.
- continuous lines: typical process (terminal temperature).
- dotted lines: process limits, bottom process limit (terminal temperature), upper process limit (top surface temperature).

III.1.3. Wave Soldering



SnAgCu and SnPb solders - Double Wave Soldering

NB: • continuous lines: typical process.
• dotted lines: process limits.

III.2. Moisture Sensitivity Classification

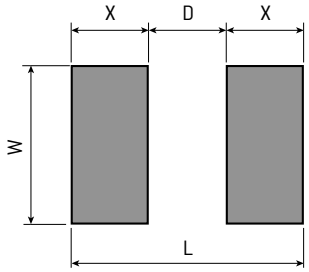
Our standard lead-free terminations - S and C types - have been fully tested and are compliant with the requirements mentioned in specification JEDEC STD 020 (level 1: not moisture sensitive).

III.3. Whiskers Classification

Our standard lead-free terminations - S and C types - have been fully tested and are compliant with the requirements mentioned in specification JEDEC STD 201. Our terminations exhibit a matte finish and receive a special heat treatment to relieve stress inside the tin.

III.4. Pad Dimensions

The metallized pads on the end user's substrate must be properly designed. Improper spacing or dimensioning of the pads may result in poor solder joints or a tombstone effect. Pad designs are given below for the most common sizes of multilayer ceramic capacitors for both wave and reflow soldering.



Case Size	W	X	D	L
SHL (0402)	0.70mm	0.90mm	0.40mm	2.20mm
CHA / SHA (0505)	1.80mm	1.00mm	0.80mm	2.80mm
SHS (0603)	1.00mm	1.10mm	0.60mm	2.80mm
SHF (0805)	1.50mm	1.30mm	0.60mm	3.20mm
CHB / SHB (1111)	3.00mm	1.00mm	1.90mm	3.90mm
CPX / CLX (2225)	6.90mm	1.00mm	5.00mm	7.00mm
CPE / CLE (4040)	10.20mm	1.10mm	8.30mm	10.50mm

NB: these dimensions are suggested for a reflow soldering process. If a wave soldering process is used, the X dimension has to be increased by 0.50mm (0.40mm for L and A case sizes), thus leading to an increase of 1.00mm to the L dimension (0.80mm for L and A case sizes).

General Information

SERIAL AND PARALLEL RESONANCE FREQUENCIES (SRF & PRF) OF CAPACITORS ON PCB

I. INTRODUCTION AND DEFINITIONS

The equivalent model for a capacitor is usually defined by the figure 1 where:

C is the capacitance of the Capacitor
RS is the equivalent serial resistance (ESR)
L is the equivalent serial inductance (ESL)
Cp is the parasitic parallel capacitance
Rp is the Insulation Resistance

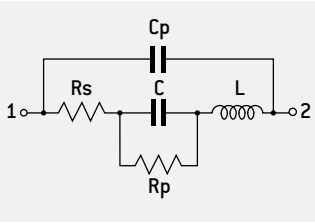


Figure 1: Equivalent Model

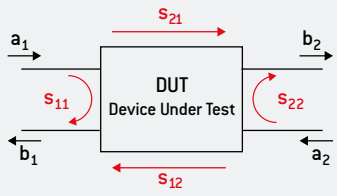


Figure 2: S parameters

The complex impedance Z is defined by:

Z=ESR + j X and z=Z/Z0 (1) where z is the reduced impedance, X the reactance, Z0 the characteristic impedance (usually 50 ohm)

The impedance can be determined by the S parameters (figure 2) measurement for example with a serial configuration (Figure 3)

$$S11 = \frac{Z}{Z+2} \quad (2)$$

$$S21 = \frac{2}{Z+2} \quad (3)$$

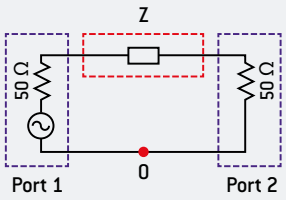


Figure 3: DUT Serial measurements

The variation of S11 (figure 4) and S21 (figure 5) show the different resonance frequencies SRF (serial resonance frequency) and PRF (parallel resonance frequency)

- The SRF is defined when the capacitor is a pure very small resistance:

$$SRF = \frac{1}{2\pi\sqrt{LC}} \quad (4a)$$

Therefore as X=0 the impedance defined in (1) is:

$$Z = ESR \quad (5)$$

At this frequency the ESR is usually low.
For example for a 251SHF150 (size 0805 and capacitance 15 pf):
SRF=2.64 GHz and the ESR at this frequency is 0.200 ohm (figure 5)

- The PRF is associated with the parasitic capacitance C_P defined in figure 1. Assuming that Cp<<C, then:

$$PRF \approx \frac{1}{2\pi\sqrt{LC_P}} \quad (4b)$$

At this frequency the impedance is a pure very high resistance.
For example for a 251SHF150:
PRF=3.66 GHz and the ESR at this frequency is very high (figure 6)
The PRF could be determined by the S21 measurements (figure 5)

The lumped model shown in Fig. 1 explains only the existence of one serial self-resonant frequency and one parallel self-resonant frequency, consequently, the lumped model is unable to explain why real measurements exhibits a double infinity of self-resonant frequencies (see figures 4, 5 & 6).

It is currently admitted [1] that the lumped model shown in Fig. 1 is convenient only for frequencies that are lower than roughly the half of the first SRF. For frequencies close or above the first SRF, it is mandatory to consider the distributed model or transmission line model [1].

This distributed model can be established more easily with the equivalent circuit of a Single Layer Capacitor (SLC) shown in Fig. 7:

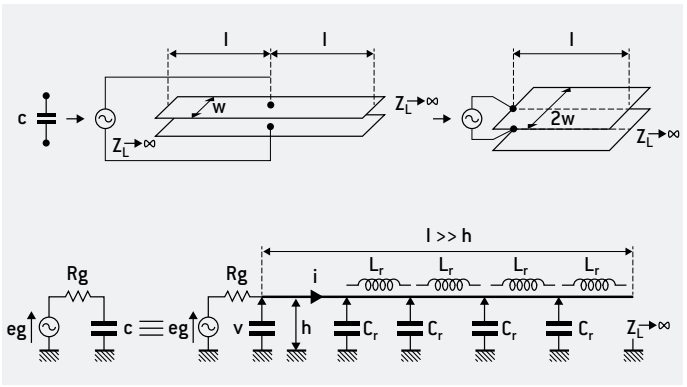


Figure 7: Transmission line model of a Single Layer Capacitor

After examination of Fig. 7, one can see that a Single Layer Capacitor can be modeled by a transmission line with an open termination that is currently called an "open stub".
According to classical courses relatives to transmission lines theory, it is well known that the variation with frequency of the input impedance of an open stub is given by:

$$Z_e = -jZ_c.\cot g\left(\frac{2\pi l}{\lambda}\right) = -jZ_c.\cot g\left(\frac{2\pi l}{c} f\right) \quad (5)$$

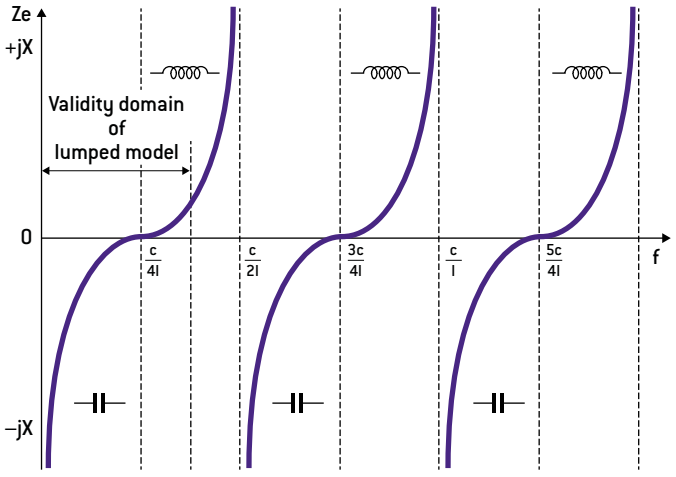


Figure 8: Plot of the theoretical expression (5) of the impedance of a Single Layer Capacitor modeled by an open stub

General Information

The plot of the theoretical expression (5) of the impedance of a Single Layer Capacitor is shown in Fig. 8. As one can see, this theoretical curve predicts a double infinity of self-resonant frequencies (alternances of serial and parallel resonances) that are identical to the ones encountered in real world measurements.
Consequently, for predicting and understanding the behavior or a capacitor at frequencies that are close or above the first SRF, the lumped model (shown in Fig. 1) is not applicable and must be replaced by the distributed model or transmission line model (shown in Fig. 7).

Furthermore, according to [1], the transmission line model predicts accurately that the serial or parallel self-resonances are doubled when a capacitor chip is mounted with its internal electrodes oriented vertically (once again, it is impossible to predict such a phenomenon with the lumped model).

If now we take a closer look at a capacitor used as a coupling capacitor in a wide band application, it is evident when looking at fig. 8 that the coupling function will be correctly fulfilled at frequencies close to the serial resonant frequencies, since the capacitor's impedance is very low.

Conversely, the contrary will be encountered at the parallel resonant frequencies since the capacitor's impedance is very high and consequently the coupling function is not fulfilled.

Therefore in the application we must avoid to be at PRF. The High ESR may involve power loss and increase of internal temperature, since:

$$P = ESR\ I^2 \quad (6)$$

$$P = \frac{\Delta T}{R_{TH}} \text{ (stationary state)} \quad (7)$$

The temperature increase is therefore:

$$\Delta T = ESR\ I^2\ R_{TH} \quad (8)$$

Where Rth is the thermal resistance of the capacitor with the PCB.

At first glance, equations (6), (7) & (8) confirm an increase of the internal temperature, but a closer look at these equations reveals that this temperature rise takes place only if the current I is constant. The problem is that in real applications the power source is rarely a pure current generator. More often than none, the power source is the dual of a current generator ie. a pure voltage generator. In the case of a circuit powered by a pure voltage generator, the contrary of the preceding behavior will be encountered at PRF since, as the capacitor's impedance is very high, the current I is very low and consequently, according to (6), (7) & (8) the temperature rise is not obvious or may be a temperature fall.

From these considerations, one can draw the conclusion that when a coupling capacitor is used at its PRF, for predicting an eventual temperature rise it is also mandatory to know for the PRF the behavior of the generator and the load between which the coupling capacitor is serially inserted.

In other words, the coupling capacitor is not the only cause of a temperature rise and consequently, the characteristics of the whole circuitry must be well known and understood prior to investigate the reasons of a temperature rise.

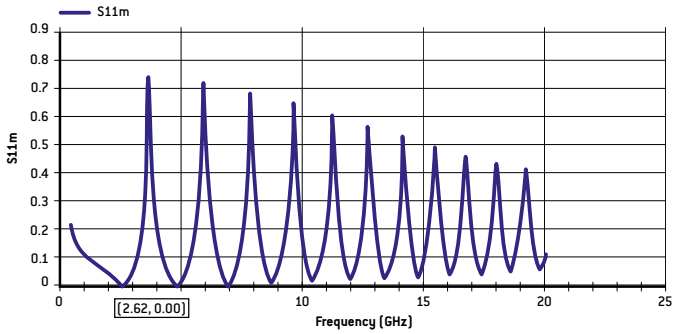


Figure 4: S11curve for a 251SHF150 from EXXELIA ABC software

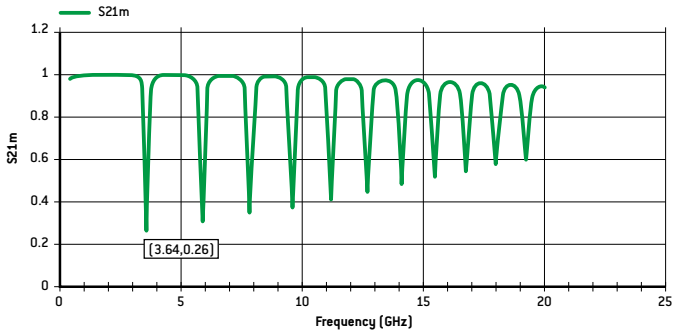


Figure 5: S21curve for a 251SHF150 from EXXELIA ABC software

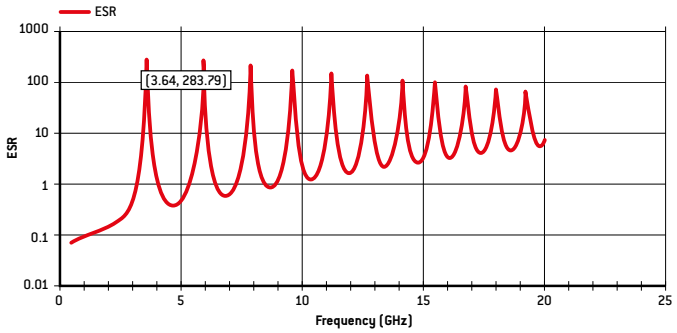


Figure 6: ESR curve for a 251SHF150 from EXXELIA ABC software

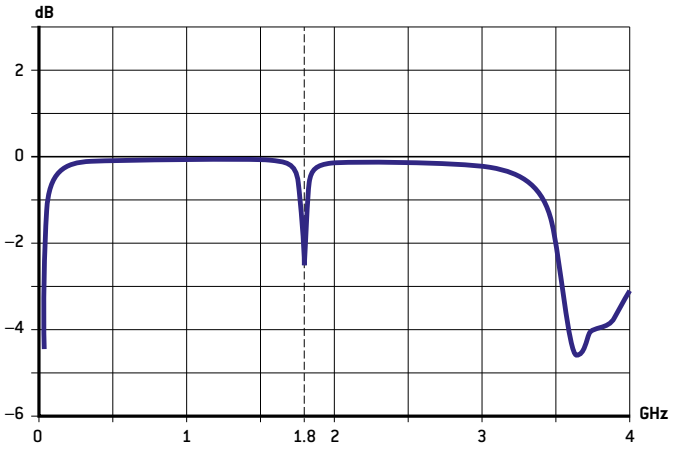
General Information

II. PARAMETERS OF SUBSTRATES AND CAPACITORS WITCH INFLUENCES THE PRF

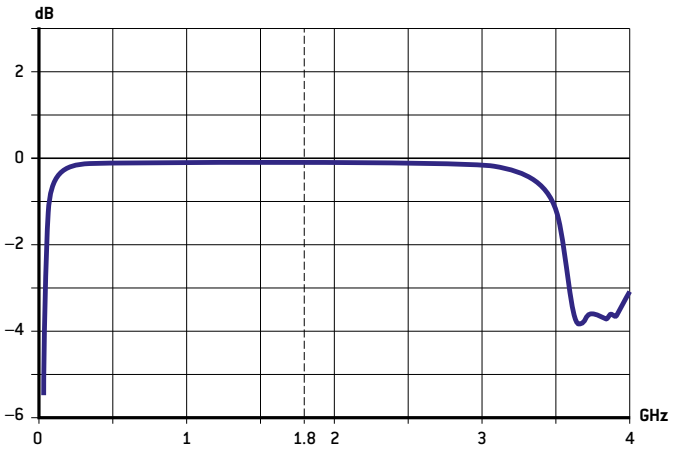
As the PRF is linked to the parasitic parallel capacitance, when the capacitor is mounted on a PCB, the main parameters witch could influence the PRF are:

- PCB parameters
- Capacitor parameters
  - Capacitance value
  - Geometry and size
  - Electrode orientation (horizontal or vertical)
  - Internal design

For example in the following screen plots, we can see that the first PRF is about 1.8GHz when the capacitor is mounted horizontally and is not visible when it is mounted vertically.



Horizontal mounting



Vertical mounting

Figure 9: Example of PRF measurement (501SHB390JS on a FR4 PCB horizontal and vertical mounting)

[1] Monolithic Capacitors as Transmission Lines. Marc INGALLS and Gordon KENT IEE Transactions on Microwaves Theory and Techniques, Vol. MTT-35, N°11 november1987, pp. 964-970.

CAPACITOR RELIABILITY DATA MIL-STD CDR STYLES, RF & AMP; MICROWAVE SYSTEMS

I. TYPICAL RELIABILITY TESTS

- Adhesive Strength of Termination
- Bending Strength
- Solderability of Termination
- Resistance to Soldering Heat
- Thermal shock −55°C to +125°C
- Humidity Load (240 hours, 85% relative humidity at +85°C)
- High Temperature Load (1000/2000h, 125°C, x U_N)

II. RELIABILITY DATA MONITORING

II.1. General Manufacturing Process

At each step of the manufacturing process, specific checks have been set-up to guarantee the quality level of our products. Statistical Process Controls (also known as SPC) are utilized to monitor key parameters within processes.

In addition to all these in-process controls, a sample of capacitors from each lot is micro-sectioned to check the internal structure and the absence of voids, delaminations, cracks or other defects.

When manufacturing is completed, the multilayer ceramic capacitors are fully screened for Capacitance, Dissipation Factor, Dielectric Withstanding Voltage, Insulation Resistance and Visual Defects.

II.2. Reliability Testing

During qualification of new capacitor series or at random intervals, Temex Ceramics performs life tests – 2,000 hours, +125°C, 2 x WVDC - and uses MIL-PRF-55681 as a guideline. The following parameters best describe our multilayer ceramic capacitors for military applications:

- data from MIL-PRF- 55681 revision F;
- capacitor, chip, multiple layer, fixed, ceramic dielectric, established reliability;
- rated temperature: −55°C to +125°C;
- CDR11, CDR12, CDR13 and CDR14 case sizes;
- Failure Rate levels C, M, P, R and S.

The data obtained from our continuous life test monitoring are used to calculate an equivalent part failure rate and to compare it to the Failure Rate level as defined in MIL-PRF-55681F. The methods and formulae used are based on MIL-HDBK217F and MIL-STD-690D.

An acceleration factor of 8:1 is used to relate life test data obtained at 200% rated voltage at maximum rated temperature, to rated voltage at maximum rated temperature (125°C). The following formula is used:

$$AF = \left(\frac{V}{V_0}\right)^3 \times 2^{\frac{T-T_0}{10}}$$

where V_0 is the rated voltage, T_0 the rated temperature, V and T the life test parameters.

III. RELIABILITY DATA SUMMARY

As stated in MIL-STD- 690D, data are accumulated from sample units selected from a production run and produced with equipment and procedures normally used in production. One of the prerequisites for valid data is that all lots produced during the production period be represented. The data are from the same product in current production, i.e. data from products of preceding designs are not acceptable.

General Information

III.1. Failure Rate Level

The summary of all collected data gives the following results:

- cumulative unit hours in millions: 9.27;
- cumulative unit hours in millions with acceleration factor: 74.16;
- number of defects: 1.

We consider a single sampling plan based on a 90 percent confidence level: FRSP-90. For this FR sampling plan, MIL-STD- 690D gives the following criteria:

FR Level Symbol	Qualified FR Level (% per 1,000 hours)	Number of Failures Permitted
C	non-ER	N/A
M	1.0	1 over 0.389M hours
P	0.1	1 over 3.89M hours
R	0.01	1 over 38.9M hours
S	0.001	1 over 389M hours

EXXELIA Temex therefore complies with the requirements of C, M, P and R failure rate levels.
S failure rate level according to European Space Agency specifications 3009/035 and 3009/036.

III.2. Mean Time To Failure

MTTF is the basic measure of reliability for non-repairable items. It is analogous to the more familiar MTBF (Mean Time Between Failures) used for systems which can be repaired and placed back in service after failure occurs. FR levels may be converted to mean time to failure (MTTF) as follows:

$$MTTF = \frac{100\,000}{FR\_level}\text{, in failure per } 10^6 \text{ hours}$$

III.3. Unit Hour Requirement

A complete Poisson distribution table is needed to compute unit hours. To calculate unit hours with a given number "C" of permitted failures (we are considering 1 permitted failure) we first have to determine the probability of acceptance P a by subtracting the FRSP value (0.90 as we have selected a confidence level of 90%) from 1.

Example: $P_a = 1 - 0.90 = 0.10$

From Poisson's table and for a Failure Rate level M, we find for the parameters "C" and P_a equal respectively to 1 and 0.10 the corresponding "m" value of 3.89; this "m" value in the table is the total of failure rate λ multiplied by the time (test hours).

$$M = \lambda \times t$$

unit hours = m ÷ λ (1%/1,000hours as we are working with FR level M)
unit hours = 3.89 ÷ 0.00001 = 0.389 million hours (around 45 years)
Values for P, R and S levels are found by multiplying the previous level by 10.

IV. PART FAILURE RATE

The Part Failure Rate as defined by MIL-HDBK- 217F is given by the following formula:

$$\lambda_p = \lambda_b . \pi_{CV} . \pi_Q . \pi_E$$

where:

- λ_b is the Base Failure Rate;
- π_{CV} is the Capacitance Factor;
- π_Q is Quality Factor;
- π_E is the Environment Factor.

The Part Failure Rate, considering the capacitor series meet the required FR level, gives the number of failures per 10^6 hours. In MIL-HDBK-217F, the values for all these parameters are given under Capacitors, Fixed, Ceramic, Temperature Compensating and Chip paragraph. The CDR style as described by MIL-PRF-55681F is taken into account and corresponds to Temex Ceramics CHA and CHB sizes.

IV.1. Quality Factor

The Quality Factor depends on the FR level. If we consider the three FR levels defined previously for Temex Ceramics multilayer capacitors, the given factors are:

Symbol	Product Level	π_Q
C	non-ER	3.0
M	1.0 % per 1,000 hours	1.0
P	0.1 % per 1,000 hours	0.3

IV.2. Environment Factor

All part reliability models include the effects of environmental stresses through the Environmental Factor. The descriptions of these environments are shown below and encompass the major areas of equipment use

Environment	Description	π_E
G_B : Ground, Benign	Non-mobile, temperature and humidity controlled environments readily accessed to maintenance; includes laboratory instruments and test equipment, medical electronic equipment, business and scientific computer complexes, and missiles and support equipment in ground silos.	1.0
G_F : Ground, Fixed	Moderately controlled environments such as installation in permanent racks with adequate cooling air and possible installation in unheated buildings; includes permanent installation of air traffic control radar and communications facilities.	2.0
G_M : Ground, Mobile	Equipment installed on wheeled or tracked vehicles and equipment manually transported; includes tactical missile ground support equipment, mobile communication equipment, tactical fire direction systems, handheld communications equipment, laser designations and range finders.	10.0

IV.3. Part Failure Rate Calculation

The part failure rate calculated as specified in MIL-HDBK-217F provides a more accurate result than the standard failure rate given by a particular FR level. The two main parameters are the FR level achieved by the standard process – Quality Factor - and the application where the part will be used – Environment Factor. Specific study could be made on request based on customer's requirements and equipments.

General Information

POWER CAPACITOR ENDURANCE TESTING ULTRA-LOW ESR, HIGH RF POWER

I. FOREWORDS

I.1. Concept

Figure 1 shows the general concept. The setup contains a direct digital synthesizer (DDS) that generates an RF signal with a variable frequency. Its signal is amplified by a driver stage followed by a power amplifier stage. The gain of the PA stage is controlled by varying its supply voltage. For that purpose a variable power supply is provided. The directional coupler measures the forward and the reflected power. The latter is a value that describes the quality of the matching condition. The role of the matching network is to match the capacitor to a 50W load. The capacitor under test is mounted on a separate printed circuit board and is encapsulated by a small cabinet. This cabinet isolates the capacitor from the ambient temperature. A temperature sensor is integrated into the cabinet to measure the capacitors temperature.

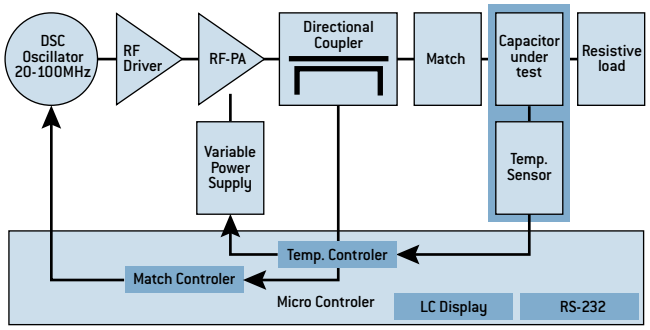


Figure 1

With a microcontroller, there are two control loops realized. The temperature of the capacitor is measured at the beginning of the 5 seconds off time with a temperature sensor. The sensor's signal is used to control the variable power supply which influences the power amplifiers gain and as a consequence, the output power or the current through the capacitor under test.

The ground plane improves the heat spread between the capacitors. This is further supported by a copper bar that is directly pressed on the ground plane of the PC board. On the front side of the copper bar, a NTC is mounted. Tests have shown that this heat coupling is very critical for the overall performance. The NTC is screwed directly and by that the heat coupling is both tight and reliable.

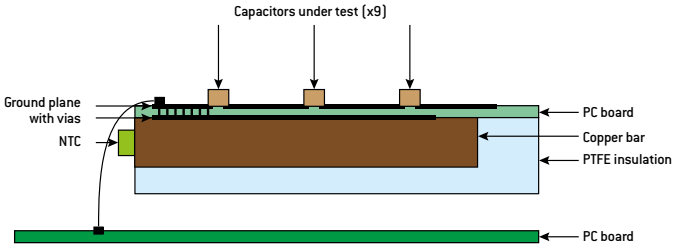


Figure 2

I.2. Test Cycle

The complete test cycle is shown in figure 3. The test starts with a tuning procedure at low power. As soon as the matching condition is achieved the RF power is set to the value that is necessary to heat the capacitors. During the ON time, the frequency is continuously adjusted to minimize the reflected power. After 5 seconds ON, the RF is switched off for the next 5 seconds. Then the RF is switched on again. Because the capacitors have cooled down during the OFF time, the test generator needs to re-tune. The re-tune procedure takes 500ms. After that, the RF is ON for the next 5 seconds. That way a complete cycle takes 10 seconds.

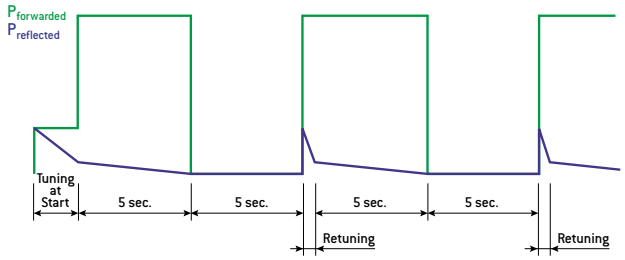


Figure 3

The following conditions have been used:

- HiQ multilayer ceramic capacitors operated at 27MHz;
- 2 complete test sets are done, one for B size (1111) and another for X size (2225);
- a complete test set represents 1 million cycles (4 months of continuous RF power).

I.3. Data Acquisition

The test generator measures continuously: the frequency, the forward power, the reflected power and the three temperatures. The test generator stores these values always at the end of the 5 seconds ON time. The remote computer gathers the data at least once each cycle and writes these records to a log file. Each file collects the record of one day and is automatically sent by email once a day.

General Information

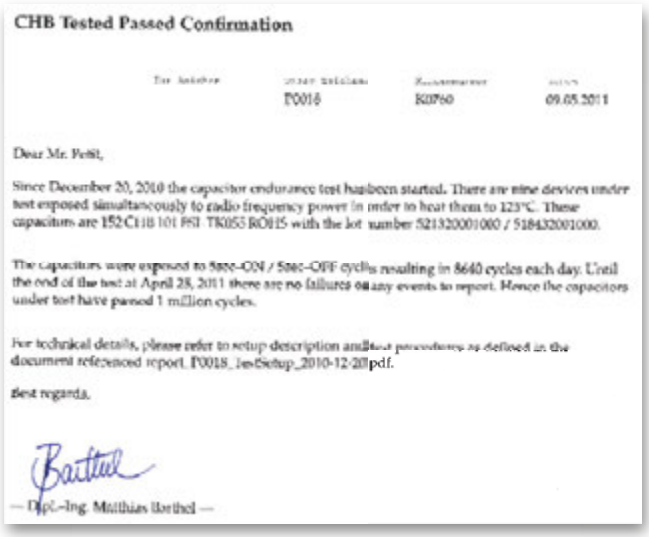
II. RESULTS

All the tests have been performed by an external independent company named Barthel HF Technik located in Aachen, Germany.

II.1. HiQ Capacitors – B Size (1111) – Solderable Nickel Barrier

The CHB series RF/Microwave capacitors offer both extended operating temperatures up to 175°C and extended voltages up to 1500 V_{DC}. These components are based on our well-known P100 HiQ dielectric, a low loss material, which is ESA and MIL qualified - ITAR free.

On May the 9th 2011, the test set was completed without any problem to report.



CHB Tested Passed Confirmation

	P0018	R0760	09.05.2011

Dear Mr. Petit,

Since December 20, 2010 the capacitor endurance test has been started. There are nine devices under test exposed simultaneously to radio frequency power in order to heat them to 125°C. These capacitors are 152 CHB 101 F6J TK055 R0415 with the lot number 521320001000 / 518432001000.

The capacitors were exposed to 5sec-ON / 5sec-OFF cycles resulting in 8640 cycles each day. Until the end of the test at April 28, 2011 there are no failures or any events to report. Hence the capacitors under test have passed 1 million cycles.

For technical details, please refer to setup description and test procedures as defined in the document referenced report P0018_TestSetup_2010-12-20.pdf.

Best regards,

Barthel

— Dipl.-Ing. Matthias Barthel —

II.2. HiQ Capacitors – X Size (2225) – Non Magnetic Solderable Barrier

The CLX series High RF Current/Voltage capacitors offer both ultra stability over temperature and extended voltages up to 3 600 V_{DC}. These components are based on our well-known NP0 HiQ dielectric, a low loss and ultra stable material, which is $MR_{certified}$® and MIL qualified - ITAR free.

On November the 9th 2011, the test set was completed without any problem to report.

CLX Test: Passed Confirmation

	P0018	R0760	22.12.2011

Dear Mr Dellacherie,

Since July 14, 2011 the capacitor endurance test has been started. There are nine devices under test exposed simultaneously to radio frequency power in order to heat them to 125°C. These capacitors are 252 CLX 101 GC ROHS with the lot number 507364001000.

The capacitors were exposed to 5sec-ON / 5sec-OFF cycles resulting in 8640 cycles each day. Until the end of the test at November 21, 2011 there are no failures or any events to report. Hence the capacitors under test have passed 1 million cycles.

For technical details, please refer to setup description and test procedures as defined in the document referenced report P0018_TestSetup_2010-12-20.pdf.

Best regards,

Barthel

— Dipl.-Ing. Matthias Barthel —

III. CONCLUSIONS

These tests have shown the reliability of Temex-Ceramics capacitors in operation. Each of the HiQ capacitors under test has been exposed during 4 months to their maximum RF power signal rating, heated up to 125°C continuously and without any failure or event to report.

This endurance test, along with the European Space Agency qualification (see ESA.pdf on our website), the regular life test performed on standard production lots (see Reliability_Data.pdf) and the MIL class R rating (see MIL.pdf) highlight, the high quality and reliability associated with Temex Ceramics capacitors.

General Information

IV. APPENDIX

The capacitance of the capacitor under test may vary during the temperature ramp up time. Additionally it may vary if there is a beginning of destruction process. If the frequency was kept constant, the RF power coupled into the capacitor under test will decrease. Hence the temperature control loop will increase the RF power.

This may lead to a situation where the temperature decreases when the RF power cannot be increased any more. In order to cope with this, there is a second control loop that varies the frequency in order to minimize the reflected power. So the RF power amplifier stage will always be able to deliver the necessary power to keep the temperature constant.

As PC board, a ceramic material from Rogers is used, the RO4350 material. Comparing to the standard FR4 material the ceramic board has the following advantages: improved heat conductivity; improved heat resistance and improved electrical strength.

Due to the improved electrical strength, it was possible to have a ground plane on the bottom side of the board. The coupler bar rests on a PTFE insulation. It was meant to be a heat insulation. However, during pre-tests, it became apparent that the PTFE material spreads the heat more than expected. In order to improve the heat insulation towards ground and the ambient air, the complete setup is now surrounded by a layer of glass wool.

All these efforts led to the following results: the temperature difference between the RF on time and the RF off time is less than 10°C and a total RF power of approximately 35 Watts is sufficient to heat the capacitors to 125°C. The capacitors under test are soldered with a non lead solder, Sn95Ag4Cu1 which has an extended temperature range also. Figure 4 shows the test setup.

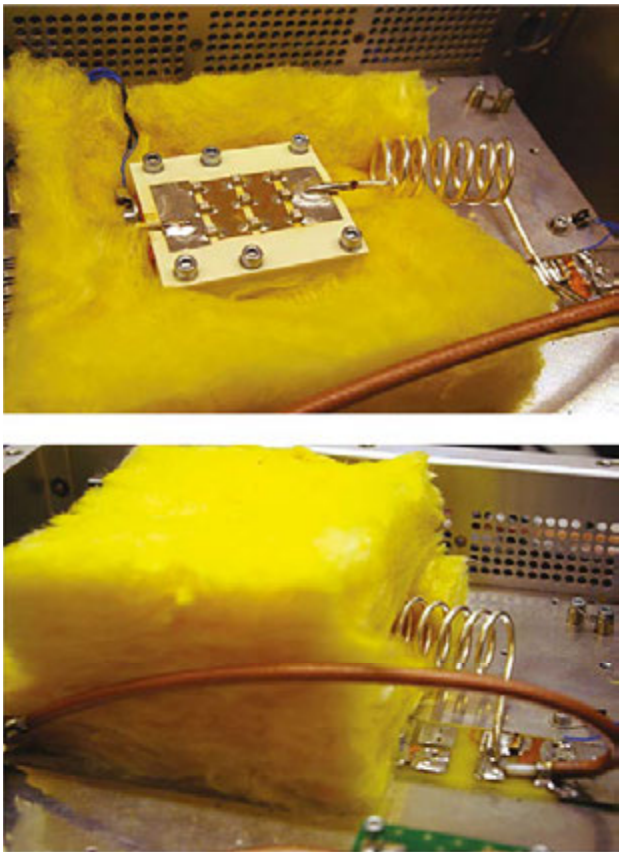


Figure 4

Both control loops are realized by a micro controller. Additionally, the micro controller provides an RS-232 interface to set some configuration values. A LC display shows warning messages also and some status information like temperature, RF power, etc.

The test generator works completely self sustained. It controls the temperature, RF power, frequency and all other parameters. The test generator takes also care that it remains itself within safe limits like maximum cool plate temperature, maximum forward power, maximum reflected power, frequency within a given bandwidth, etc. The test generator is connected to a remote computer.

Reverse Geometry

SHR / SHD Series

FEATURES

- Reverse-Geometry MLCC providing Ultra low ESL and very High Self Resonant Frequencies
- High power dissipation
- Lowest ESR in class, RF & Microwave capacitors
- Working voltage: 500V
- Sizes: 0709 and 0711
- Capacitance range: 0.5pF - 100pF
- NP0, RoHS compliant
- Operating temperature up to 175°C
- Laser Marked (optional)

APPLICATIONS

- Cellular Base Station Equipments
- Broadband Wireless Service
- Point to Point / Multipoint Radios
- Broadcasting Equipment

CIRCUIT APPLICATIONS

- Impedance Matching
- Bypass, Feedback
- Tuning, Coupling and DC Blocking

PHYSICAL CHARACTERISTICS

Chip capacitors for surface mounting with Nickel barrier and tinning.

ELECTRICAL AND ENVIRONMENTAL SPECIFICATIONS

Electrical specifications	
Parameter	**Value**
Capacitance	0.5pF - 100pF
Tolerances	A, B, C, D below 10pF F, G, J, K above 10pF
Working voltage (WVDC)	500V
Temperature coefficient	NP0: (0 ± 30) ppm/°C, −55°C to +175°C
Insulation Resistance	10^5 MΩ min.
Dielectric Withstanding (test voltage applied for 5 seconds)	1,250V
Aging	none
Piezo Effect	none

Environmental specifications	
Parameter	**Value**
Life Test	2,000 hours, +125°C at 1,000V 1,000 hours, +175°C at 500V
Moisture Resistance Test 1	240 hours, 85% relative humidity at 85°C (ESA/SCC n°3009)
Moisture Resistance Test 2	56 days, 93% relative humidity at 40°C 0V, 5V, WVDC

HOW TO ORDER

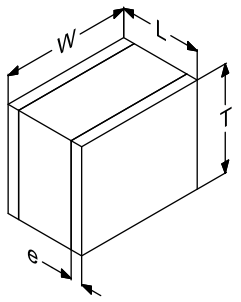
501	SH	R	100	J	S	L	E	-RoHS
Voltage code	Dielectric	Size code	Capacitance code	Tolerance code	Termination code	Marking code	Tape and reel	
501 = 500V	**SH** = NP0: (0±30) ppm/°C	**R** = 0709 **D** = 0711	Please refer to Cap. Code given in capacitance range chart	**A** = ±0.05pF **B** = ±0.1pF **C** = ±0.25pF **D** = ±0.5pF **F** = ±1% **G** = ±2% **J** = ±5% **K** = ±10% See note	**S** = Standard: tin-plated nickel All terminations are backward compatible and lead-free	**-**: no marking **L** = laser marking	**-**: no tape and reel **E** = Tape and reel packaging Number of components per reel: 1,000.	The RoHS tag is not part of the reference Tag added at the end of P/N for information

Note: For capacitance values less than 3.3pF, tolerances A, B, C and D are available. For capacitance values less than 10pF, tolerances B, C and D are available. For capacitance values of 10pF or higher, tolerances F, G, J and K are available. Please consult us for specific requirements.

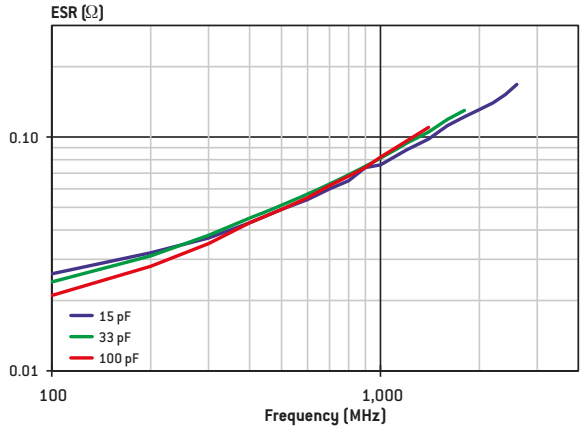
SHR / SHD Series

Reverse Geometry

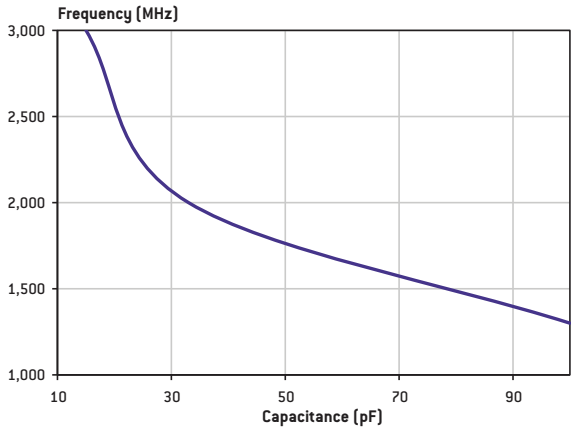
DIMENSIONS in inches (mm)



TYPICAL ESR VERSUS FREQUENCY



TYPICAL SERIES RESONANT FREQUENCY VERSUS CAPACITANCE



STANDARD RATINGS

Size		0709	0711
Size code		R	D
Dimensions inches (mm)	L	0.07 ± 0.015 (1.78 ± 0.38)	0.07 ± 0.015 (1.78 ± 0.38)
	W	0.09 ± 0.01 (2.29 ± 0.25)	0.105 ± 0.01 (2.67 ± 0.25)
	T	0.106 max (2.67 max)	0.09 max (2.29 max)
	e	0.01 +0.008/-0.006 (0.25 +0.2/-0.15)	0.01 +0.008/-0.006 (0.25 +0.2/-0.15)
Value (pF)	Cap. Code	Standard	Standard
0.5	0R5		
0.6	0R6		
0.7	0R7		
0.8	0R8		
0.9	0R9		
1.0	1R0		
1.1	1R1		
1.2	1R2		
1.3	1R3		
1.4	1R4		
1.5	1R5		
1.6	1R6		
1.7	1R7		
1.8	1R8		
1.9	1R9		
2.0	2R0		
2.1	2R1		
2.2	2R2		
2.4	2R4		
2.7	2R7		
3.0	3R0		
3.3	3R3		
3.6	3R6		
3.9	3R9		
4.3	4R3		
4.7	4R7		
5.1	5R1		
5.6	5R6		
6.2	6R2	500V	500V
6.8	6R8		
7.5	7R5		
8.2	8R2		
9.1	9R1		
10	100		
11	110		
12	120		
15	150		
16	160		
18	180		
20	200		
22	220		
24	240		
27	270		
30	300		
33	330		
36	360		
39	390		
43	430		
47	470		
51	510		
56	560		
62	620		
68	680		
75	750		
82	820		
91	910		
100	101		